WBS 6.5.1.1: Tile Calorimeter Main Board

- Need to deliver 1200 Main boards to CERN
  - 100 in pre-production, 1100 in production (described in BOE)
- WBS includes R&D activities:
  - several design tweaking iterations (incorporate info from tests)
  - radiation certification of components
  - construction of “module zero” to refine firmware, calibrations, etc
- Head engineer has important role in Tile upgrade
  - needs to spend time at CERN (“expert weeks”, training, meetings)
- Pre-production sets up the assembly line structure
  - and construction of burn-in benches, equipment, etc.
- Production done in 5-week cycles (80 boards ea)

Costing Details: Components

- We have the Bill of Materials from prototype production
- We have quotes for PCB assembly in various lot sizes
- Propose to purchase all passive components in 1 lot for volume discount
  - More expensive IC's assuming 20% discount
- Summary of cost per Main Board (1100 needed; 100 preproduction):

Item:	Quantity of 100	Quantity of 550
Passive components	$96.23	$96.23
IC's	$704.38	$563.50
PCB	$400.00	$240.00
Assembly	$190.20	$182.00
total	$1,390.81	$1,081.73

Costing Details: Production Labor

- BOM, negociate discounts and special lots: EE
- Parts packages, short-test PCB: ET
- Oversee PCB assembly, initial testing, debugging with assy house: EE, ET
- Mount in burn-in fixtures; supervise students: EE, ET, UG
- Diagnose and repair failures; document: EE, ET
- Inventory, crate and ship to CERN: ET
- Acceptance test training at CERN and system integration meetings: EE

FTE Summary: 2.44 EE, 1.08 ET, 2.27 Undergraduate Students for production phase

LRS Structure: Rates

- Fully burdened rates. No IDC on engineers; 58% on undergrads

FTE	hours/year	1760
Inflation	percent/year	3.00%

UC rates given to Chuck 5/18/2016 and inflated by him to start 10/1/2016
hrs/yr changed from 1776 to 1760

Inst/Position	Base Cost (k$/year – burdened)	FTE Rate FY17	FY18	FY19	FY20	FY21	FY22	FY23	FY24
UChicago									
Electronics Engineer		186.5	192.1	197.8	203.8	209.9	216.2	222.7	229.3
IT Engineer		142.1	146.3	150.7	155.3	159.9	164.7	169.7	174.7
Electronics Technician		115.4	118.9	122.5	126.1	129.9	133.8	137.8	142.0
Undergrad student		38.6	39.8	41.0	42.2	43.4	44.8	46.1	47.5

Travel for 1-week trip to CERN based on much experience;

1 week at CERN:		
7d	transportation	1800
	Foyer	560
	Meals	210
total w/IDC	K$	**3.86**

LRS Structure: Labor FTE

MAB		workdays	Travel	Matl	Equip	EE hrs	EA hrs	ET hrs	STU hrs
1380	START: pro								
1390M	order/stock passives, some ICs	60	0	883860		160		160	
1400	expert weeks	30	15420	0		40		0	
1410M	PCB assy: 1st 40	20	50	7280		80		35	
1420	BTR 1st 40	20	0	0		160		48	280
1430	ship 1st 40	5	0	1704		0		35	
1440	Test, training @ CERN	10	5140	0		80		0	
1450	PCB assy 80x13	260	650	189280		1040		455	
1460	BTR 80x13	260	0	0		2080		624	3640
1470	ship 80x13	65	0	22152		0		455	
1890	PCB assy 20	20	50	3640		20		35	
1900	BTR 20	20	0	0		40		12	70
1910	ship 20	5	0	1704		0		35	
1920	COMP: Production								
1930	testing,QA@CERN	101	10280	0		600		0	
	totals	876	31,590	1,109,620	0	4,300	0	1,894	3,990
	FTE					2.44	0.00	1.08	2.27

Some Labor Calculations

- PCB assembly: This involves significant testing and debugging to set up board stuffing at vendor. ET receives raw PCBs, inspects visually and performs tests for shorts; sends boards and parts packs to vendor. Based on demonstrator experience, EE spends 1-2 weeks with vendor to set up assembly machine. Upon receiving assembled boards, EE and ET perform visual inspection and testing for shorts before attaching leads and powering up.
- Burn-in: FEB are attached to MBs and monitored for 5d while operating at elevated temperature. There are 5 burn-in fixtures, each containing 4 MB; amounts to 2,200 total hours of testing. EE overseas this critical operation; ET mounts boards into fixtures, stores tested boards, and keeps an eye on the students. Students monitor the data acquisition, start/end testing cycles, and analyze and log the data. They also run calibrations and linearity tests on the FEBs.
  - 20% of EE overseeing, keeping records, reporting to management
  - 60% of ET conducting the process (essentially full-time during the course of each 30 week run)
  - 1 FTE undergraduate (done by 4 or 5 students) during each run
  - matches well with what was needed 1999-2000 for burn-in of legacy motherboards
- Repair: experience from the demonstrator and in-general: 10% of the boards will need attention. Diagnosis is done by EE. Difficult repairs are done by EE and take half a day on average (demonstrator). Simple (connector) problems fixed by ET: about 25% of boards, 1 hour each. Amounts to 20% each EE,ET.
- Shipping: Paperwork, crating, monitoring shipment = 1 week of ET
- Acceptance and management: the head EE is essential to the project; needs to attend 4 expert weeks/yr

Compare to 1997 Cost Book

U.S. ATLAS
WBS Summary Cost Estimates

Funding Source: All **Funding Type:** All 12/22/97 12:32:26 PM

- UChicago produced the legacy Motherboard + Digitizer: similar burn-in task
  - EE: 1512 hr
  - ET: 1568 hr
  - SRA: 3552 hr (this would be an ET in current proposal)
  - Undergrads: 3552 hr
    - conversion: FTE = 1776 hr
- Total for production of 1128 boards: 5.8 FTE
  - cf: 5.2 in this proposal

Schedule compares well to 2001-3

similar task to produce “motherboards”

Shpmnt	Boxes	MB1	MB2	MB3	MB4	Mezz.	DateShipped	DateReceived
1	1	1	1	1	1	1	6-Jun-01	
2	4	4	4	4	4	4	15-Jun-01	
3	1	1	1	1	1	1	25-Jun-01	
4	1	6	6	6	6	6	5-Jul-01	11-Jul-01
5	1	3	3	3	3	3	18-Jul-01	
6	3	17	17	17	17	17	30-Oct-01	1-Nov-01
7	4	29	29	29	29	29	30-Nov-01	5-Dec-01
8	1	8	8	8	8	8	30-Jan-02	5-Feb-02
9	12	48	48	48	48	48	26-Feb-02	8-Mar-02
10	4	16	16	16	16	16	29-Mar-02	
11	5	20	20	20	20	20	10-Apr-02	
12	8	32	32	32	32	32	26-Apr-02	
13	8	42	42	42	42	42	31-May-02	3-Jun-02
14	3	12	12	12	12	12	27-Jun-02	2-Jul-02
15	3	12	12	12	12	12	29-Jul-02	1-Aug-02
16	1	4	4	4	4	4	31-Jul-02	2-Aug-02
17	2	8	8	8	8	8	26-Aug-02	3-Sep-02
18	1	4	4	4	4	4	30-Sep-02	7-Oct-02
19	1	0	0	0	0	4	31-Jan-03	18-Feb-03
20	2	9	9	9	9	9	8-May-03	14-May-03
						Delta days:	701	
						cycle days	35.05	